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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,897	10/30/2003	Seok-Woo Lee	053785-5158	5713
9629	7590	06/16/2005	EXAMINER	
MORGAN LEWIS & BOCKIUS LLP 1111 PENNSYLVANIA AVENUE NW WASHINGTON, DC 20004			GUERRERO, MARIA F	
			ART UNIT	PAPER NUMBER
			2822	

DATE MAILED: 06/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/695,897

Applicant(s)

LEE, SEOK-WOO

Examiner

Maria Guerrero

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 25 April 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

### **DETAILED ACTION**

1. This Office Action is in response to the Election and the amendment filed April 25, 2005.

### **Status of Claims**

2. Claims 1-12 are pending.

### ***Election/Restrictions***

3. The Election/Restriction mailed March 25, 2005 has been withdrawn in view of the amendment filed April 25, 2005.

### ***Priority***

4. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### ***Information Disclosure Statement***

5. The information disclosure statement (s) filed October 30, 2003 and February 16 2005 have been considered.

### ***Claim Objections***

6. Claims 2, 5 and 12 are objected to because of the following informalities: the term "polysilicon" is misspelled in claim 2, line 18. Claim 5 recites "y" in line 3. Claim 12 recites "the protuberances of the polysilicon layer"; it is suggested to replace "according to claim 2" by – according to claim 11-. Appropriate correction is required.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takemura (US 5,534,716) in view of Applicant admitted prior art.

Takemura shows forming a buffer layer on a transparent substrate, forming an amorphous silicon layer on the buffer layer, and crystallizing the amorphous silicon layer (Abstract, col. 6, lines 15-40, col. 8, lines 26-47). Takemura discloses patterning the crystallized silicon layer to form an active layer (col. 6, lines 47-60, col. 8, lines 52-55). Takemura teaches performing a rapid thermal annealing (RTA) process to the active layer in an atmosphere comprising hydrogen (col. 8, lines 57-61). Takemura describes performing a rapid thermal oxidation (RTO) process under an oxygen-based atmosphere (O<sub>2</sub>) at a temperature of 550 to 650 degrees Celsius to form a silicon-oxidized layer on the active layer after the RTA process (col. 3, lines 27-35, col. 6, lines 65-67, col. 7, lines 1-5, col. 9, lines 12-22).

In addition, Takemura shows forming a metal layer (aluminum) over the transparent substrate to cover the silicon-oxidized layer and patterning the metal layer to form a gate electrode over the active layer (col. 9, lines 13-40). Takemura discloses doping the active layer with impurities using the gate electrode as a doping mask to form ohmic contact regions (col. 9, lines 47-62). Takemura teaches forming an

interlayer insulator (silicon oxide) over the transparent substrate to cover the gate electrode and patterning the interlayer insulator to form first and second contact holes exposing the ohmic contact regions (col. 10, lines 10-16).

Furthermore, Takemura describes forming source and drain electrodes on the interlayer insulator contacting the ohmic contact regions (Fig. 4F, 6F, 7F). Takemura shows forming a passivation layer on the interlayer insulation to cover the source and drain electrodes and forming a pixel electrode contacting the drain electrode through the drain contact hole (4F, 6F, 7F, col. 8, lines 3-11, col. 10, lines 10-16).

Takemura is silent about using the sequential lateral solidification (SLS) method to form the polysilicon layer. Takemura is silent about patterning the silicon-oxidized layer into the same shape as the gate electrode and protuberances being generated during the crystallizing step. However, Applicant admitted prior art shows crystallizing the amorphous silicon layer into a polysilicon layer by the sequential lateral solidification (SLS) method (pages 2-6). Applicant admitted prior art also shows that protuberances are generated during the crystallizing step (page 15). Applicant admitted prior art describes patterning the silicon-oxidized layer into the same shape as the gate electrode and forming the pixel electrode on the passivation layer contacting the drain electrode through the drain contact hole (Fig. 1A-4, pages 13-16).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Takemura's process by including the teachings of Applicant admitted prior art such as the sequential lateral solidification (SLS) method to

Art Unit: 2822

form the polysilicon layer in order to obtain a polysilicon layer having large grains and to obtain a TFT device having low leak current.

### **Conclusion**

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Yamazaki et al. (US 6,168,980), Suzuki (US 6,569,716), Kunii (US 6,569,720) and Takemura (US 6,479,331) teach several embodiments pertinent to applicant's disclosure.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Maria Guerrero whose telephone number is 571-272-1837.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

June 10, 2005

*Maria Guerrero*  
**MARIA F. GUERRERO**  
**PRIMARY EXAMINER**